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ELECTRONIC OPTICAL PROCESSOR

Abstract: This article discusses one of the most important problems of performance limitation in electronic systems, named interconnection scalability. Several theories have been put forward to solve this problem. The most probable ways of solving it are also considered.

Key words: interconnections, optoelectronics, superconductors, computer systems.

Digital processing of information requires nonlinear devices and circuits for logical functions and storage, and also interconnections to carry the information from one place to another. The continuing exponential reduction in feature sizes on electronic chips, known as Moore's law, leads to ever larger numbers of faster devices at lower cost per device. This evolution is shifting the balance between devices and interconnection in digital processing systems; electrical interconnections, at least as we know them today, do not scale to keep up with the devices. Problems with scaling electrical interconnections have been known for some time, at least implicitly. For example, essentially all telecommunications has moved away from electrical lines for long-distance traffic because the loss at high frequencies in electrical wires is too high. Also, inside computer systems, the buses that carry information from one part of the system to another run at rates much slower than the clock rate on the chips because of a variety of problems with electrical interconnects, including wave reflections on the lines.

The existence of interconnect scaling problems has been highlighted recently because of the roadmaps created by the Semiconductor Industry Association (SIA). These roadmaps show that even on semiconductor chips themselves, where interconnects are short, plentiful, and inexpensive by any absolute measure, the global interconnects will become very difficult. It is already the case for electrical interconnections between chips

that the performance is dominated by the interconnection medium rather than the devices at either end; once, in the next decade, this will also be the case for many connections on chips [2].

There are several possible approaches to such interconnection scaling problems, and and they are likely to be used to some extent. Architectures could be changed to minimize interconnection. Design approaches could put increasing emphasis on the interconnection layout. Signaling on wires could be significantly improved though the use of a variety of techniques, such as equalization. Most important for this discussion is a fourth approach—changing the physical means of interconnection.

Optics is arguably a very interesting and different physical approach to interconnection that can in principle address most, if not all, of the problems encountered in electrical interconnections. It should be emphasized here that the difficulties of electrical interconnections are not simply ones of scaling of the raw capacity of the interconnection system. There are a variety of other difficulties that are not so readily quantified but that in the end could be dominant reasons for changing to a radical solution like optics. This includes issues such as voltage isolation, timing accuracy, and overall ease of design. The design issue might turn out to be an important one; for example, an electrical bus designed for 500 MHz may well not work at 600 MHz because of different loss, inductance, crosstalk, and wave reflection phenomena. By contrast, an optical system designed for 500 MHz might continue to work equally well up to 500 GHz (if we had the devices to drive and receive the optical signals) because the frequency of modulation has essentially no effect on the propagation of the light signals.

There are other possible physical approaches to improving electrical interconnections, including cooling the chips and/or circuits (to get lower resistance in lines), e.g., to 77 K, or using superconducting lines. Cooling to low room temperatures is already implemented in some computers. Cryogenic cooling would be physically possible with current technology. Superconducting materials are still not available for room temperature, and so the use of superconductors would also require significant cooling; unless temperatures 77 K are used, relatively novel, practical, high-temperature superconductor materials would have to be developed. The number of metal levels can be increased, with seven levels apparently currently in production, and larger numbers of levels under development. There is significant cost to developing further levels, and it is not clear that

this is a scalable solution to interconnect problems in the long run. It is also possible to consider using off-chip wiring layers attached to the chip to augment the on-chip wiring [1].

There is, however, an underlying scaling difficulty with electrical interconnections, which limits both on-chip and off-chip wiring even if we have the ability to make many layers. One interesting approach is to stack chips in a three-dimensional structure with appropriate vertical connections. This approach may well help, though power dissipation can become a problem in such approaches because the surface area is not increasing significantly as chips are stacked. This power dissipation increase may to some extent be offset by the opportunity to use shorter interconnections in such a 3-D structure. Even such 3-D structures do not avoid some of the underlying scaling limits of electrical interconnections. In addition, all of these electrical approaches do not address the other qualitative problems like voltage isolation, timing accuracy, and ease of design. Thus, in general, though there are other approaches to electrical interconnect that may well help, there are underlying scaling issues and other physical problems that remain.

Implementing optical interconnects to chips would also face many technical challenges. If we wish seriously to impact interconnections on-chip or chip-to-chip, we need to be considering technologies that can allow "dense" optical interconnects at the chip level, by which we mean at least hundreds or more likely thousands or more of optical interconnects for each chip. Without such numbers, most off-chip interconnects and long on-chip interconnects would have to remain electrical.

Much sophisticated optical and optoelectronic technology has been developed for long-distance communications, but the requirements of dense interconnects are substantially different. Low power dissipation, small latency, small physical size, and the ability to integrate with mainstream silicon electronics in large numbers are all required for dense interconnects at the chip-to-chip or on-chip level. Existing optical telecommunications applications do not require any of these constraints, and the technologies developed do not satisfy them. Additionally, the discrete approaches used for long distances are likely not to be viable for dense interconnects [3].

There are, however, other opportunities in optical and optoelectronic technology that have been researched over the last several years that are apparently capable of operating at the densities needed, though the

technologies are often quite different from those of long-distance communications and are much less mature.

So the main problem is the scalability of electrical interconnections in electronics. In connection with the high complexity of using superconducting lines, the most rational solution will be the transition from electronics to optics in interconnections.

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ЭЛЕКТРОННО-ОПТИЧЕСКИЙ ПРОЦЕССОР

Аннотация: в данной статье рассмотрена одна из самых главных проблем ограничения быстродействия современных электронных систем, а именно проблема масштабируемости межсоединений. Выдвинуты несколько теорий по решению данной проблемы, а также рассмотрены самые вероятные способы ее решения.

Ключевые слова: межсоединения, оптоэлектроника, сверхпроводники, компьютерные системы.

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